CLAIMS

What is claimed is:

1. A universal Reed-Solomon (R-S) decoding integrated circuit (IC) for correcting errors in a received data bit stream signal having a selectable data width and a selectable data block size, comprising:

a configuration control means;

a data input means;

a configurable computational processing means, further comprising:

a plurality of configurable arithmetic-operation blocks;

a plurality of configurable interconnections between the configurable arithmetic-operation blocks; and

an error identification means;

an error correction means; and

a data output means.

2. The universal R-S decoding IC according to Claim 1, wherein the configuration control means comprises a plurality of user input parameters.

3. The universal R-S decoding IC according to Claim 2, wherein the configuration control means comprises a means for implementing one data width configuration from a plurality of data width configurations.

4. The universal R-S decoding IC according to Claim 2, wherein the configuration control means comprises a means for implementing one data block size from a plurality of data block sizes.

5. The universal R-S decoding IC according to Claim 2, wherein the configuration control means comprises a means for inputting scalar coefficients.

6. The universal R-S decoding IC according to Claim 1, wherein each one of the plurality of configurable arithmetic-operation blocks further comprises a plurality of logical circuit gates needed to implement one or more of the mathematical operations from the group consisting of addition, multiplication, and inversion.

7. The universal R-S decoding IC according to Claim 6, wherein each one of the a plurality of configurable arithmetic-operation blocks has a configuration control receiving means, a data signal input means, a computation means, an error-correction means, and a data signal output means.

8. The universal R-S decoding IC according to Claim 7, wherein the configurable computational processing means is configured by the loading of one or more coefficients from the configuration control means.

9. The universal R-S decoding IC according to Claim 1, wherein the configurable computational processing means is characterized in that hardware for a first Galois field can perform mathematical operations on a second Galois field.

10. The universal R-S decoding IC according to Claim 1, wherein the error identification mean computes the error location and magnitude in an inputted data block.

11. An integrated circuit (IC) for correcting data errors using a Reed-Solomon (R-S) decoder, comprising at least a first selectable computational processor and a second selectable computational processor and a configuration control means for selecting one and only one of the computational processors.

12. The IC according to Claim 11, wherein the first and the second computational processors each comprise a data signal input means, a computation means, an error-correction means, and a data signal output means.

13. The IC according to Claim 12, wherein the first computational processor has a plurality of mathematical functions required to implement a first Reed-Solomon decoder for a data signal having a first width, and the second computational processor has a plurality of mathematical functions required to

implement a second Reed-Solomon decoder for a data signal having a second width.

14. The IC according to Claim 13, wherein the first width comprises 8 bits and the second width comprises 7 bits.

15. The IC according to Claim 11, wherein the configuration control means further comprises:

a user command input means;

a first selection means for logically selecting one or more arithmetic functional blocks from a plurality of arithmetic functional blocks to realized the Reed-Solomon decoder; and

an outputting means for configuring the IC according to the selection means.

16. A method for selecting a unique set of electronic decoder elements from a plurality of decoder elements in an integrated circuit (IC) to implement one Reed-Solomon Decoder from a plurality of possible Reed-Solomon (R-S) decoders, comprising the steps of:

a) loading a Galois field symbol size parameter into the IC;

b) loading a plurality of multiplier coefficients into the IC;

c) loading a data block size parameter n into the IC; and

d) loading a parity symbol width size parameter into the IC.

17. The method according to Claim 16, wherein the Galois field symbol size parameter comprises 7 or 8 bits.

18. The method according to Claim 16, wherein the plurality of multiplier coefficients are characterized in that a particular R-S polynomial is implemented in the IC.

19. A method for correcting data errors in a serial data block using an integrated circuit (IC) having a configurable Reed-Solomon (R-S) error-correction decoder, comprising the steps of:

a) loading a plurality of configuration parameters into the IC;

b) inputting a first data block into the IC;

c) processing the data block in the configured IC to identify and enumerate any data errors in the data block;

d) outputting a corrected data block if the number of errors are below a predetermined threshold; or

e) outputting an error signal if the number or errors exceeds the predetermined threshold.

20. The method according to Claim 19, wherein the data block comprises a portion relating to data and a portion relating to parity checking.